

FIG. 1

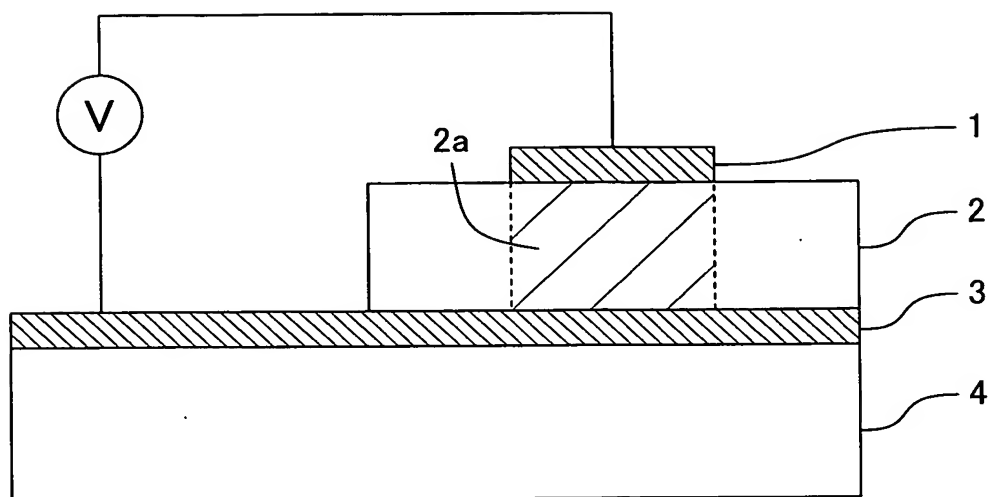


FIG. 2

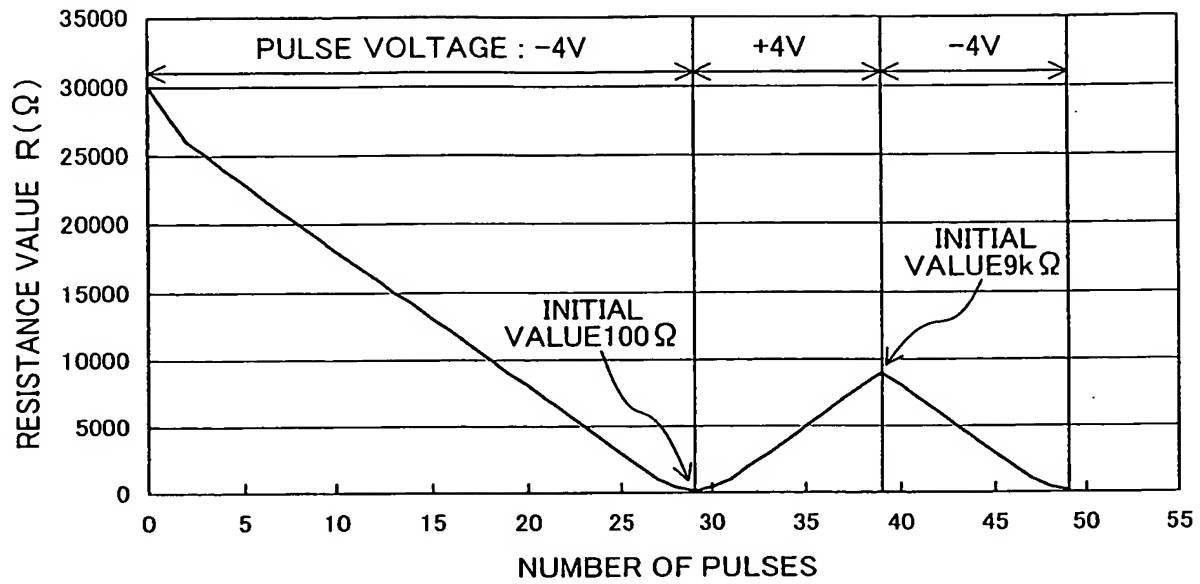
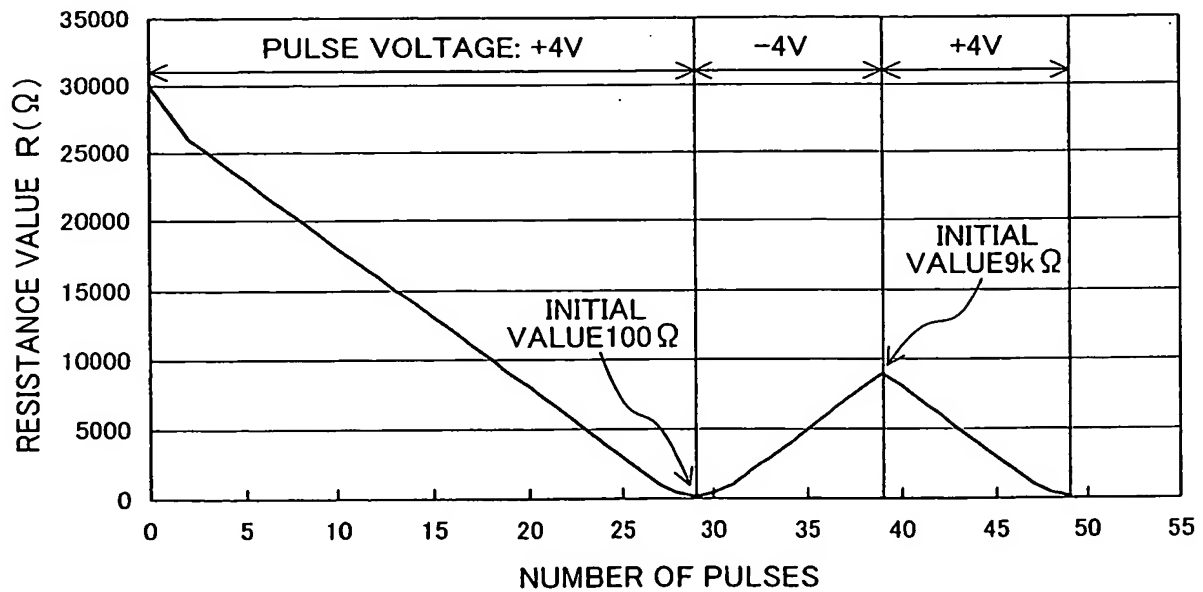
(a) VARIABLE RESISTOR  $\alpha$ (b) VARIABLE RESISTOR  $\beta$ 

FIG. 3

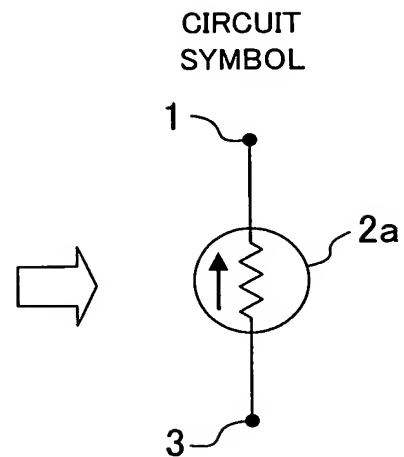
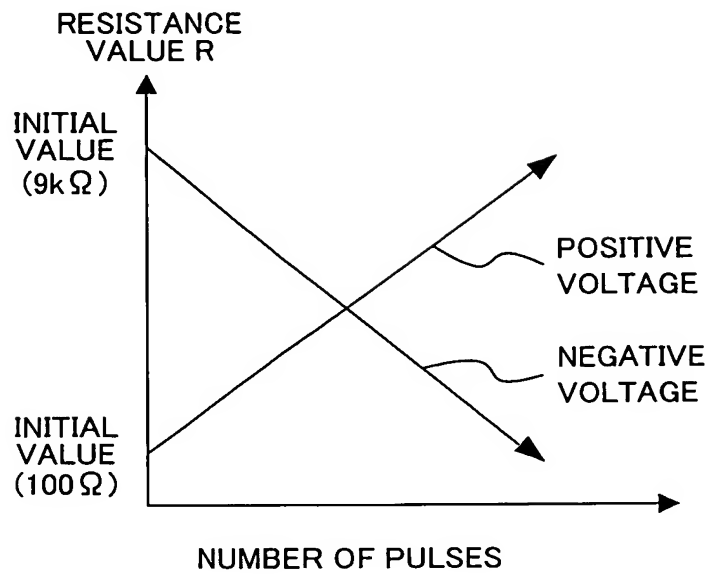
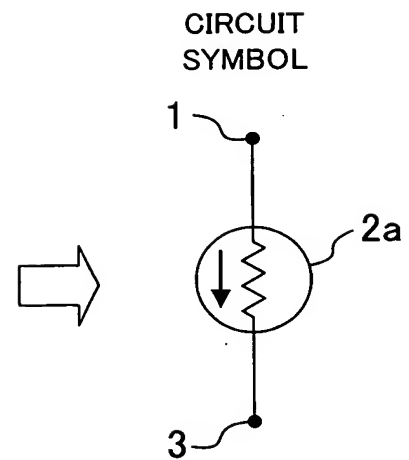
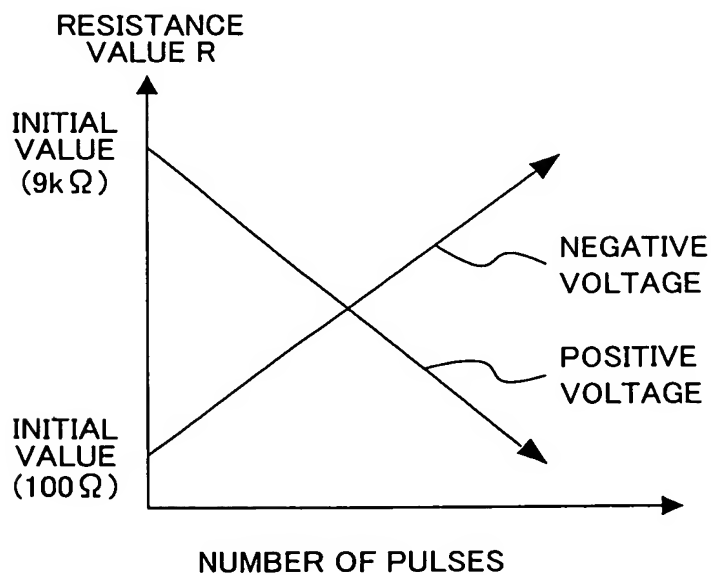
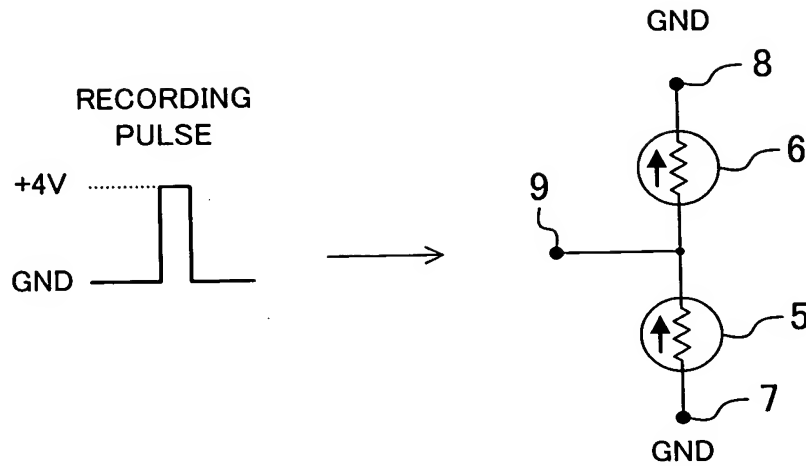
(a) VARIABLE RESISTOR  $\alpha$ (b) VARIABLE RESISTOR  $\beta$ 

FIG. 4

(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR

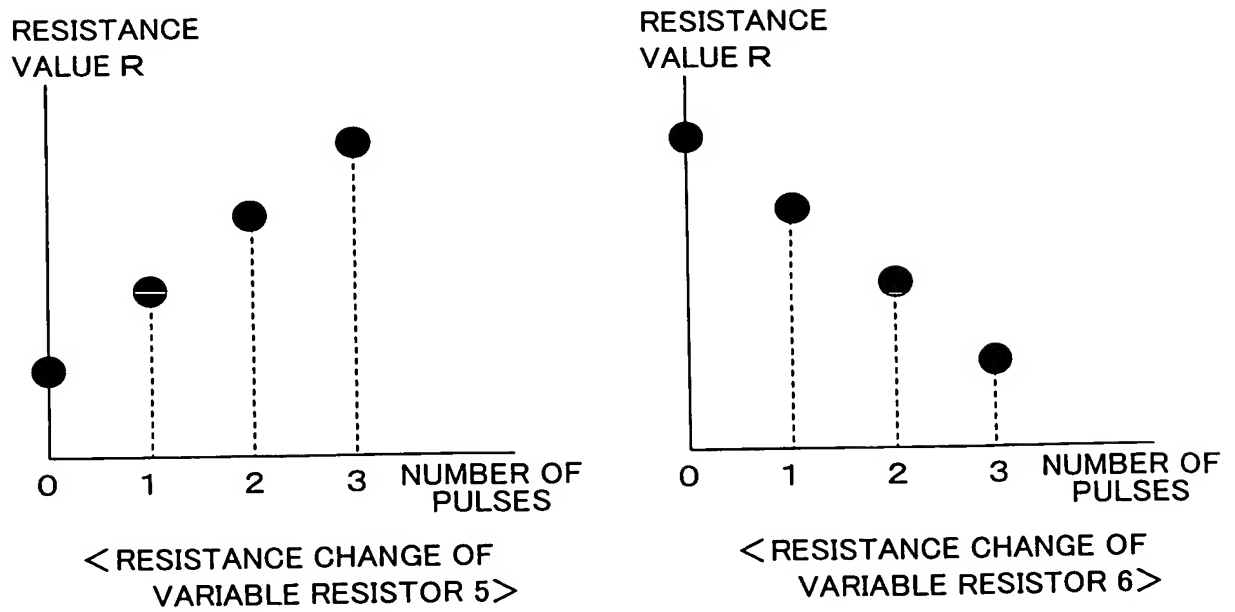
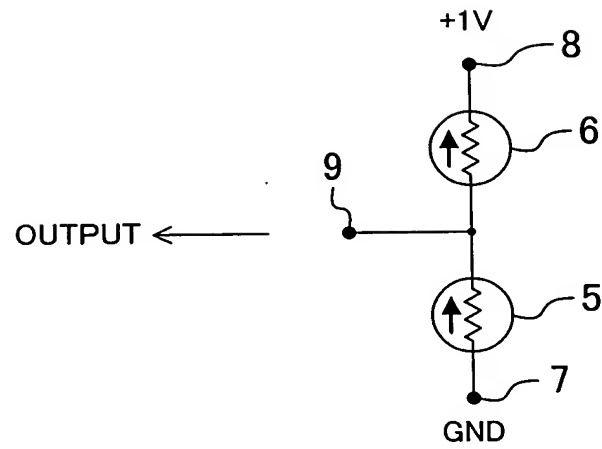


FIG. 5

(a) REPRODUCTION



(b) REPRODUCTION OUTPUT VOLTAGE

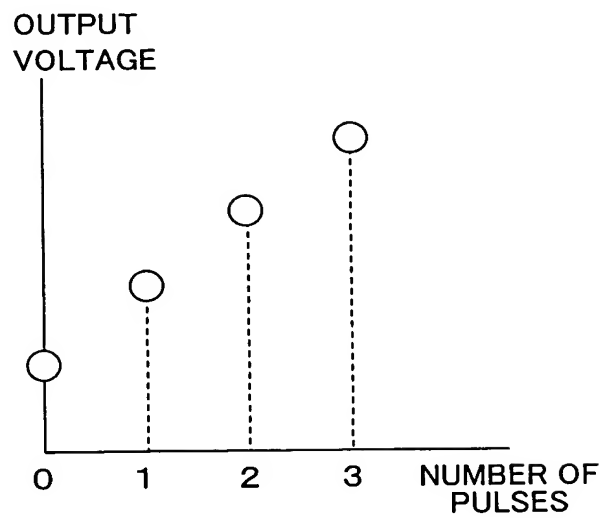
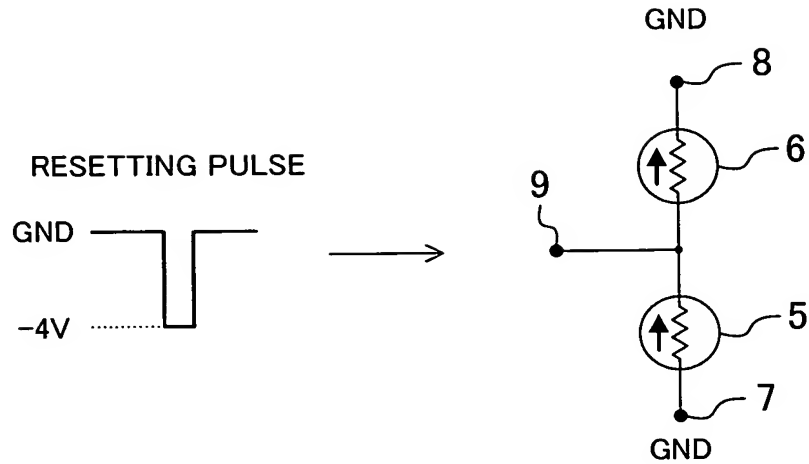


FIG. 6

## (a) RESETTING



## (b) RESISTANCE CHANGE OF VARIABLE RESISTOR

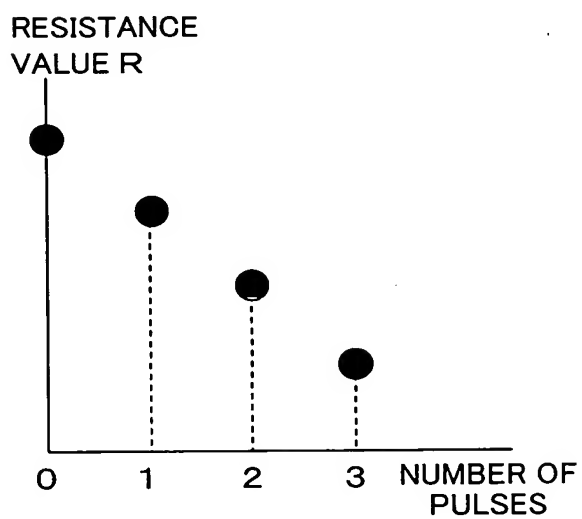
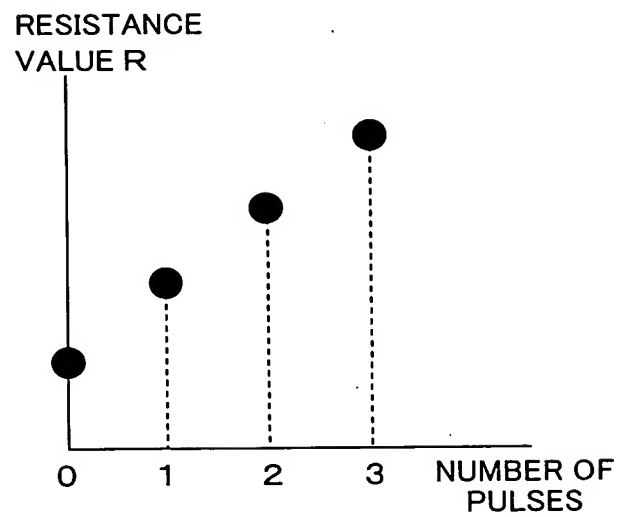
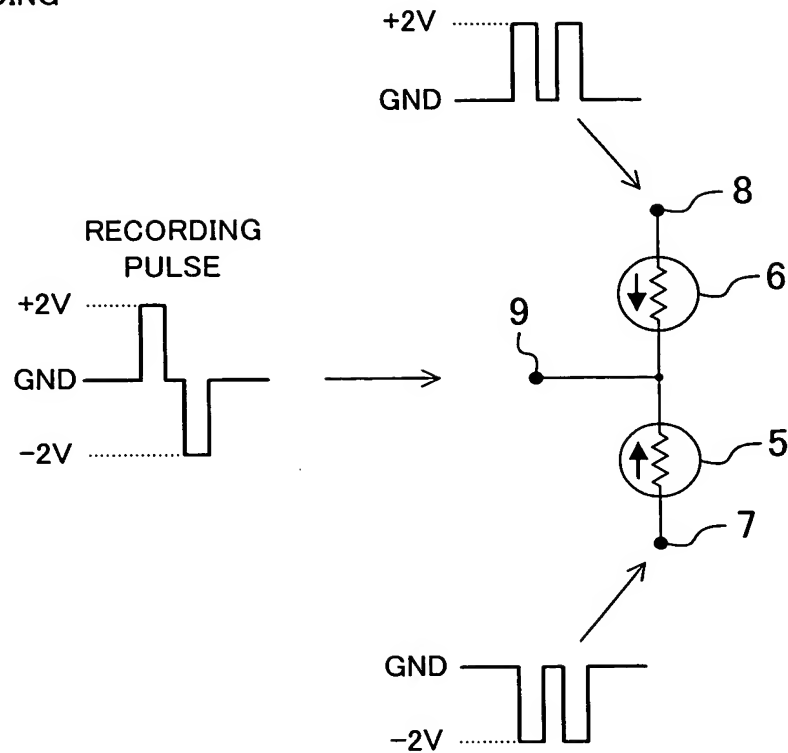
< RESISTANCE CHANGE OF  
VARIABLE RESISTOR 5 >< RESISTANCE CHANGE OF  
VARIABLE RESISTOR 6 >

FIG. 7

(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR

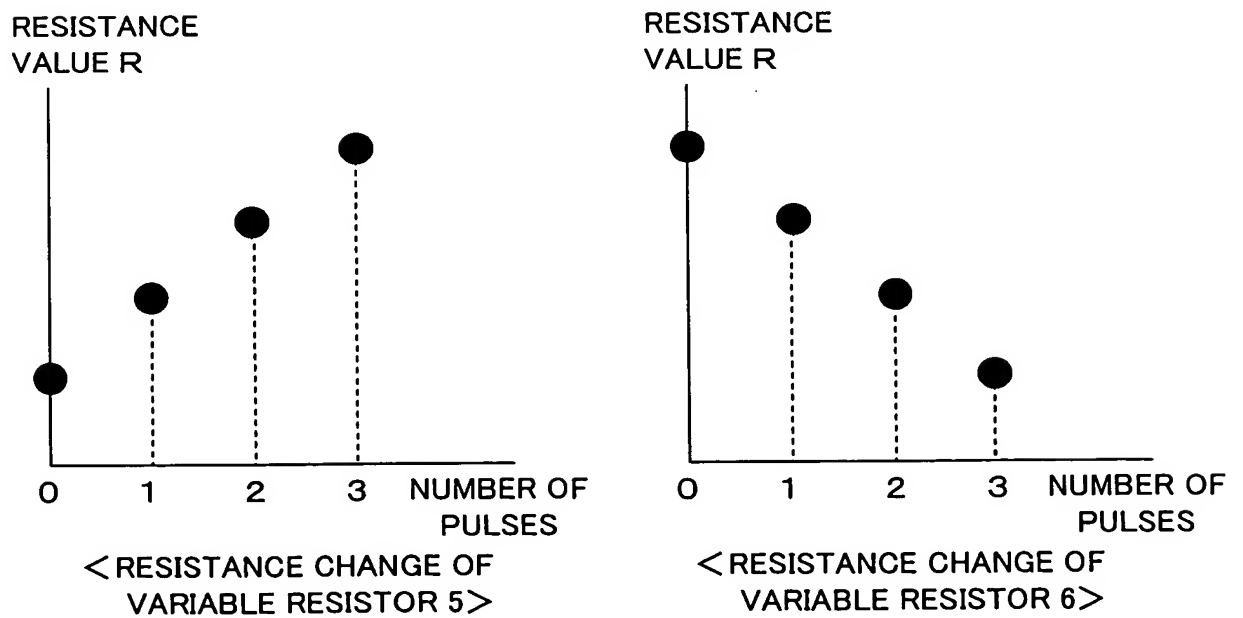




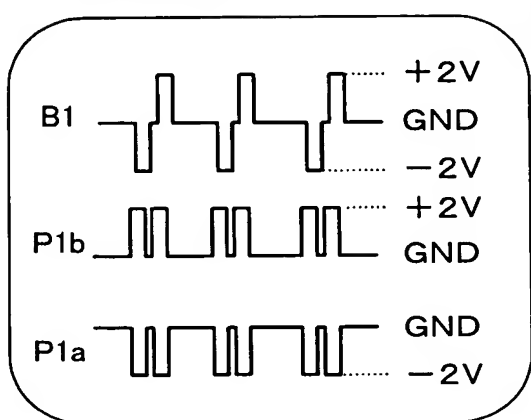




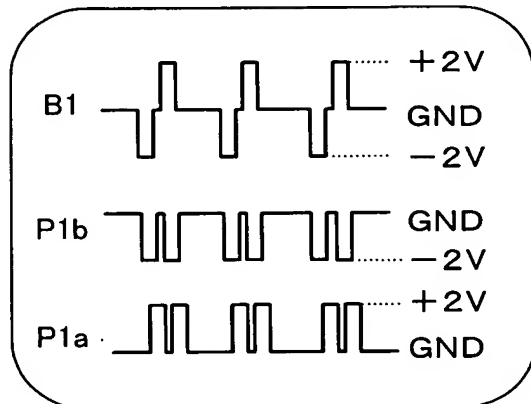
FIG. 10

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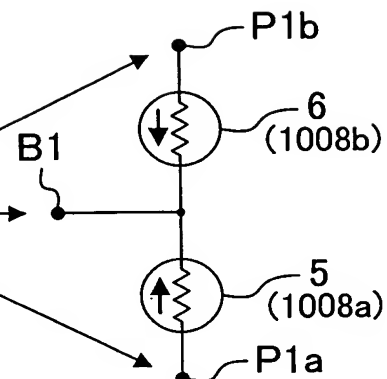
(a) RECORDING



RESETTING



ELECTRICAL PULSE



(b)

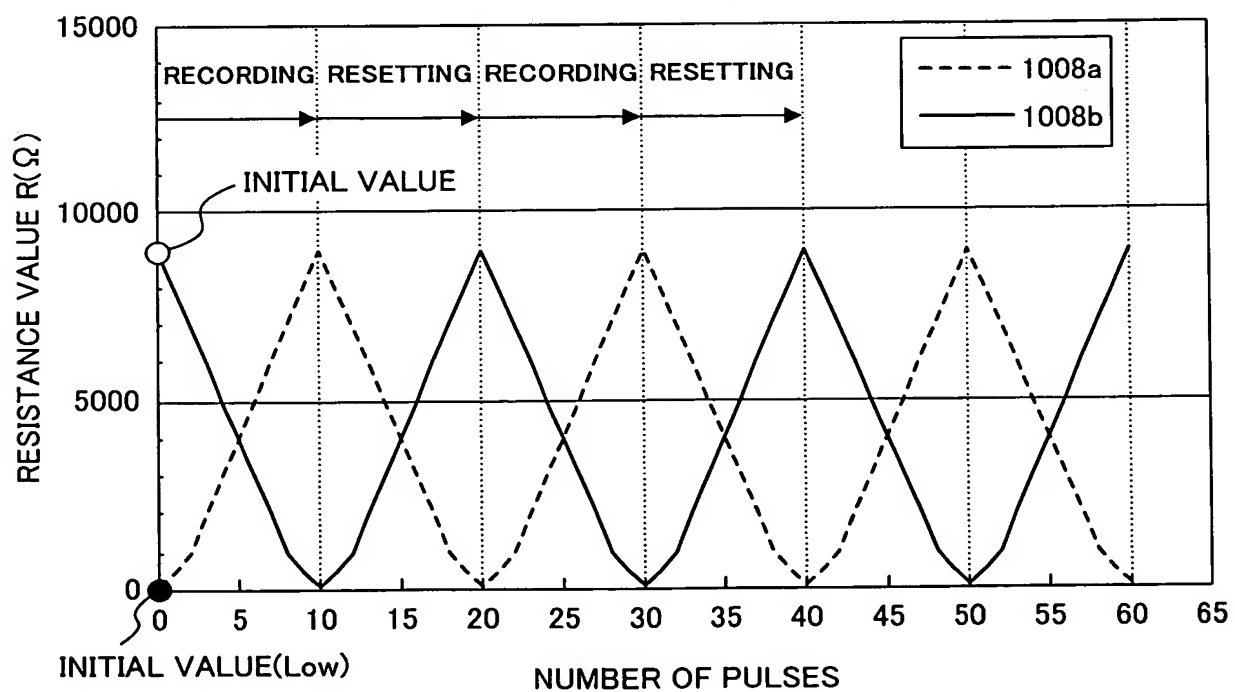
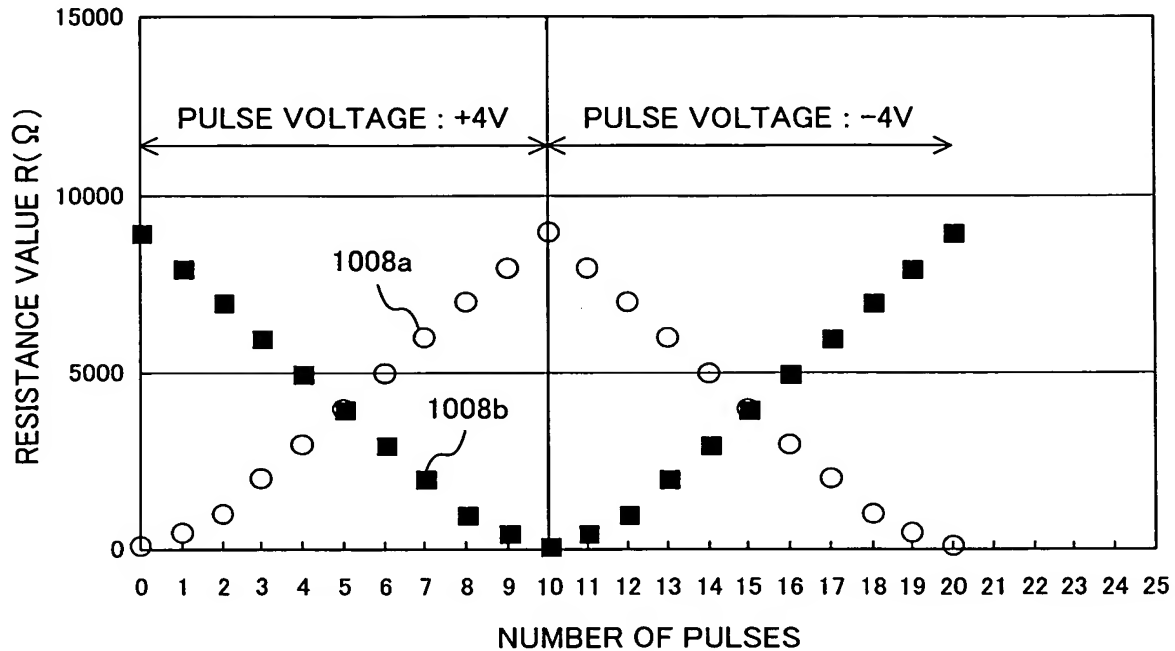


FIG. 11

## (a) RESISTANCE CHANGE WITH NUMBER OF PULSES



## (b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

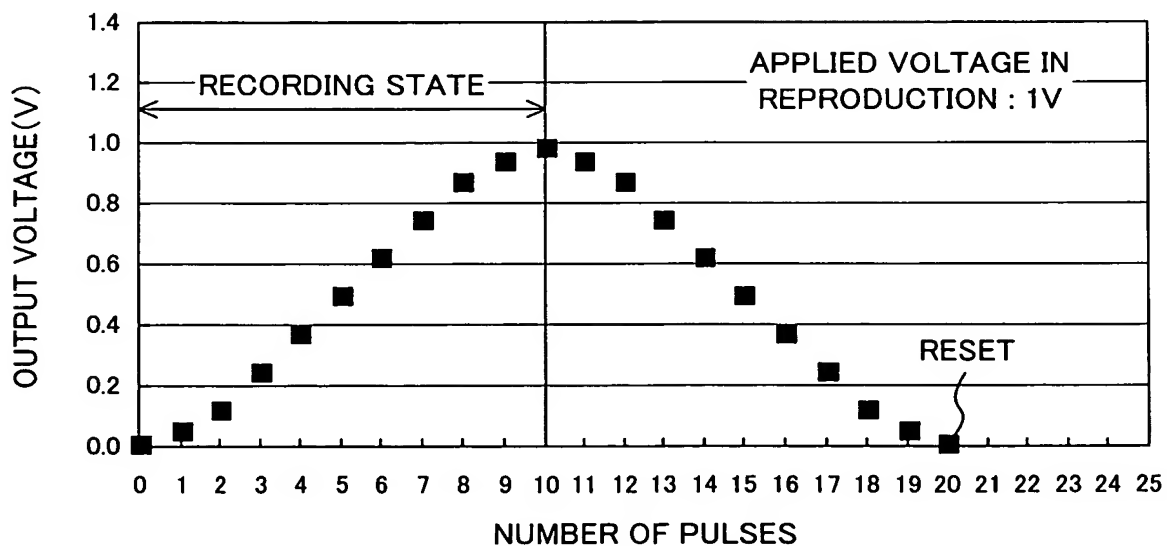
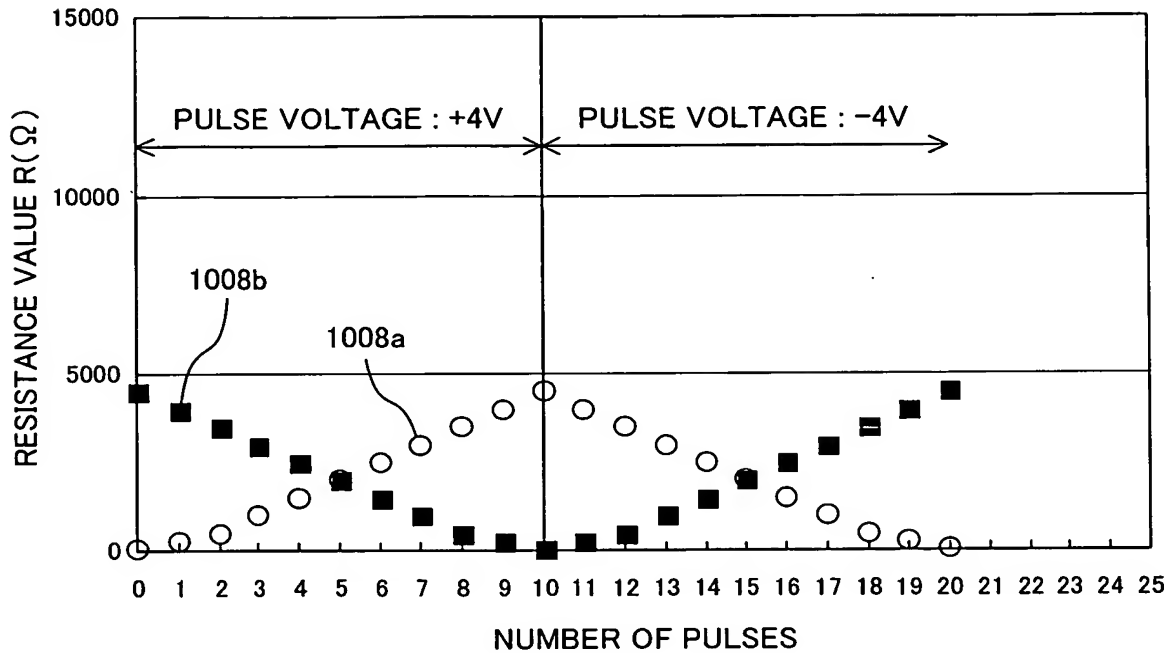


FIG. 12

(a) RESISTANCE CHANGE WITH NUMBER OF PULSES



(b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

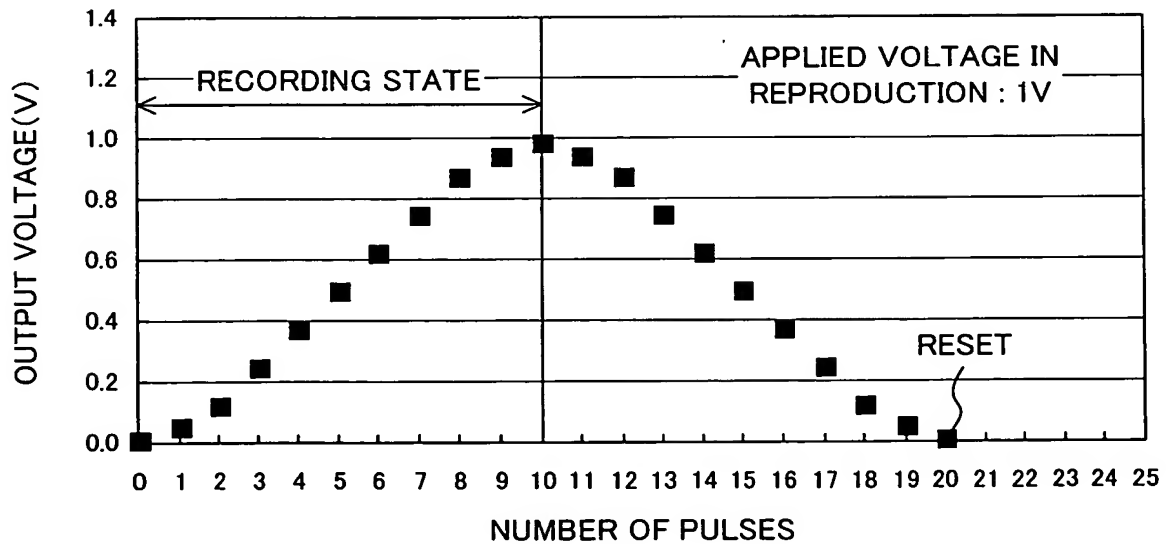


FIG. 13

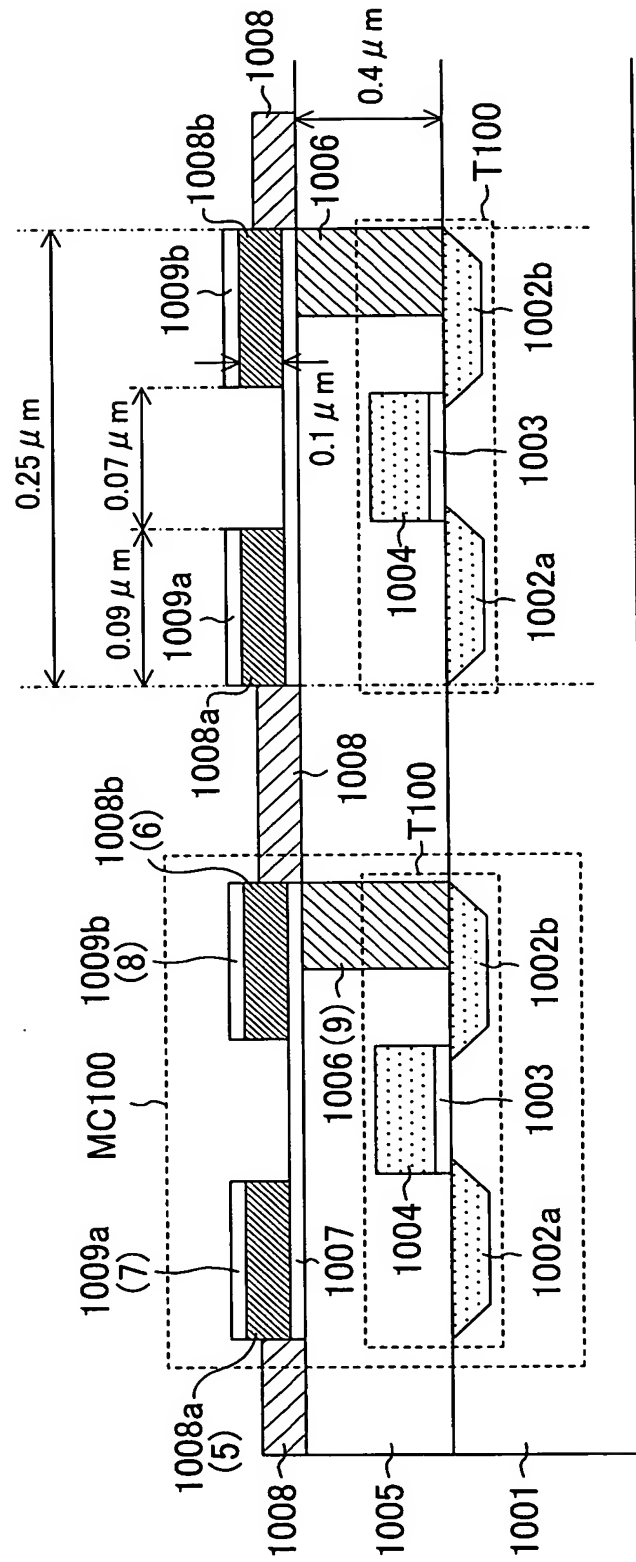


FIG. 14

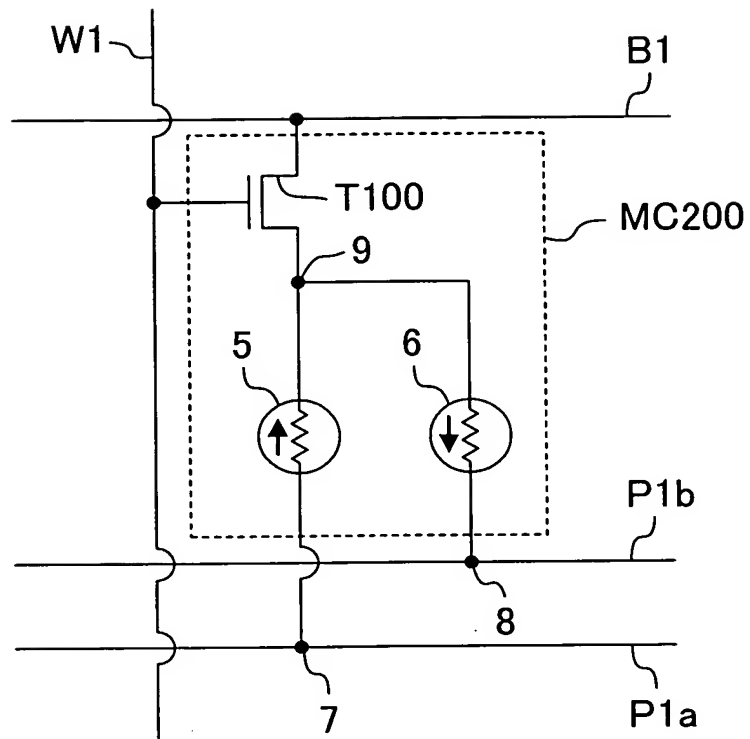
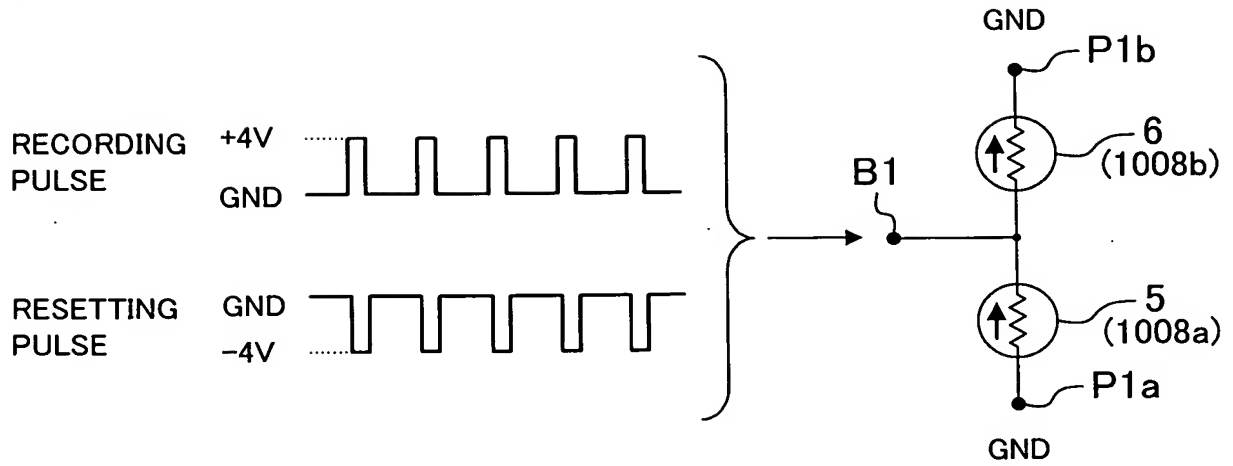
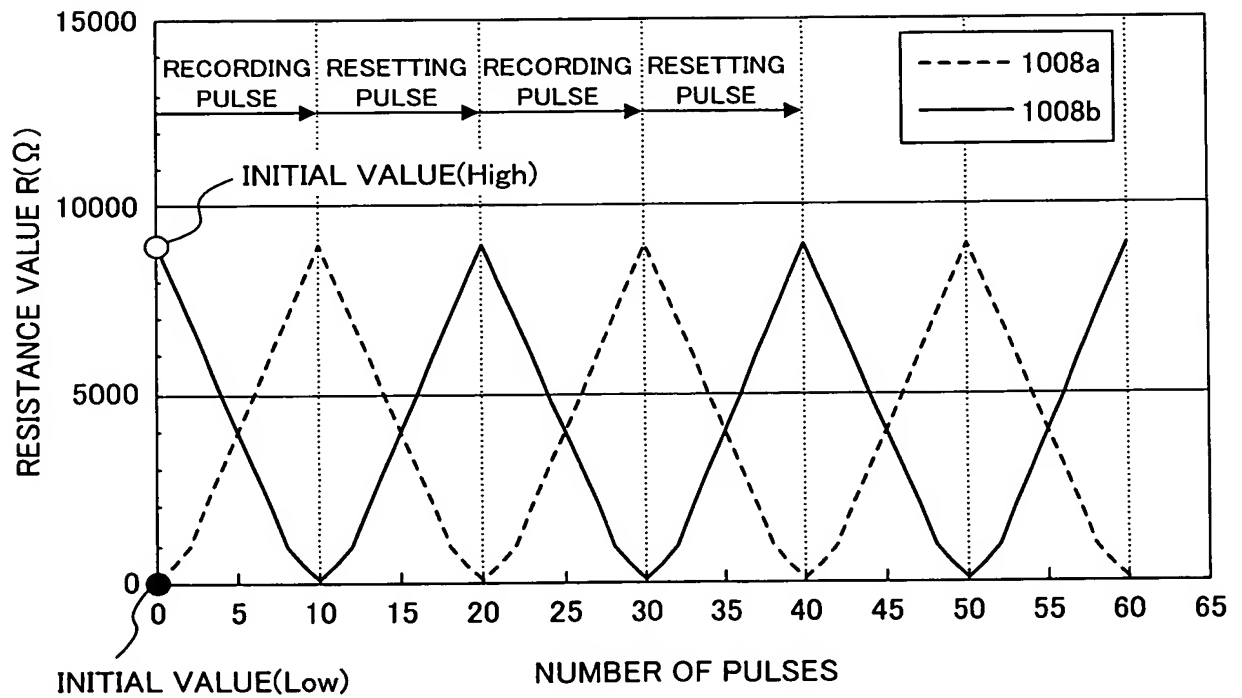


FIG. 15

(a)



(b)



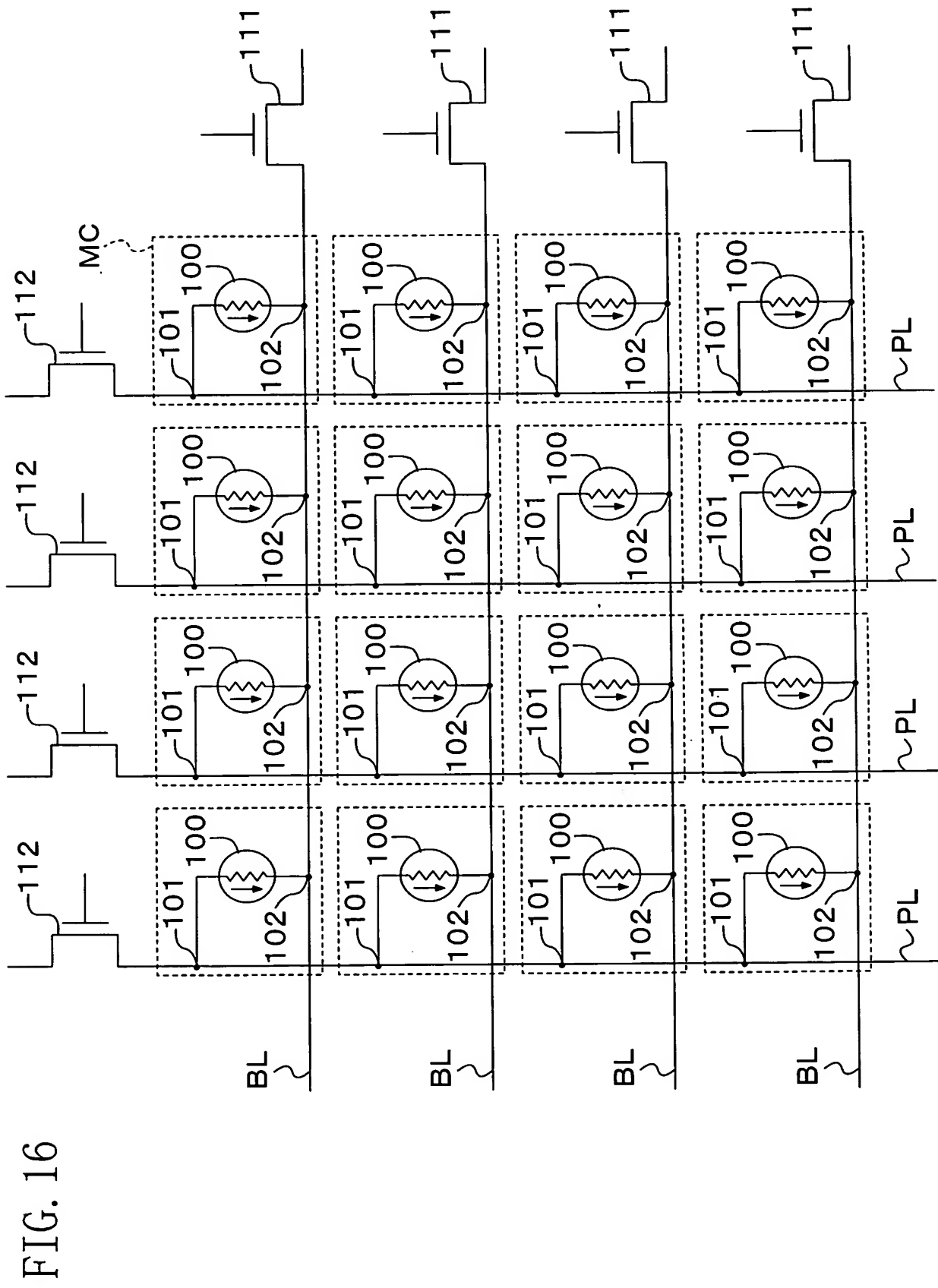




FIG. 17

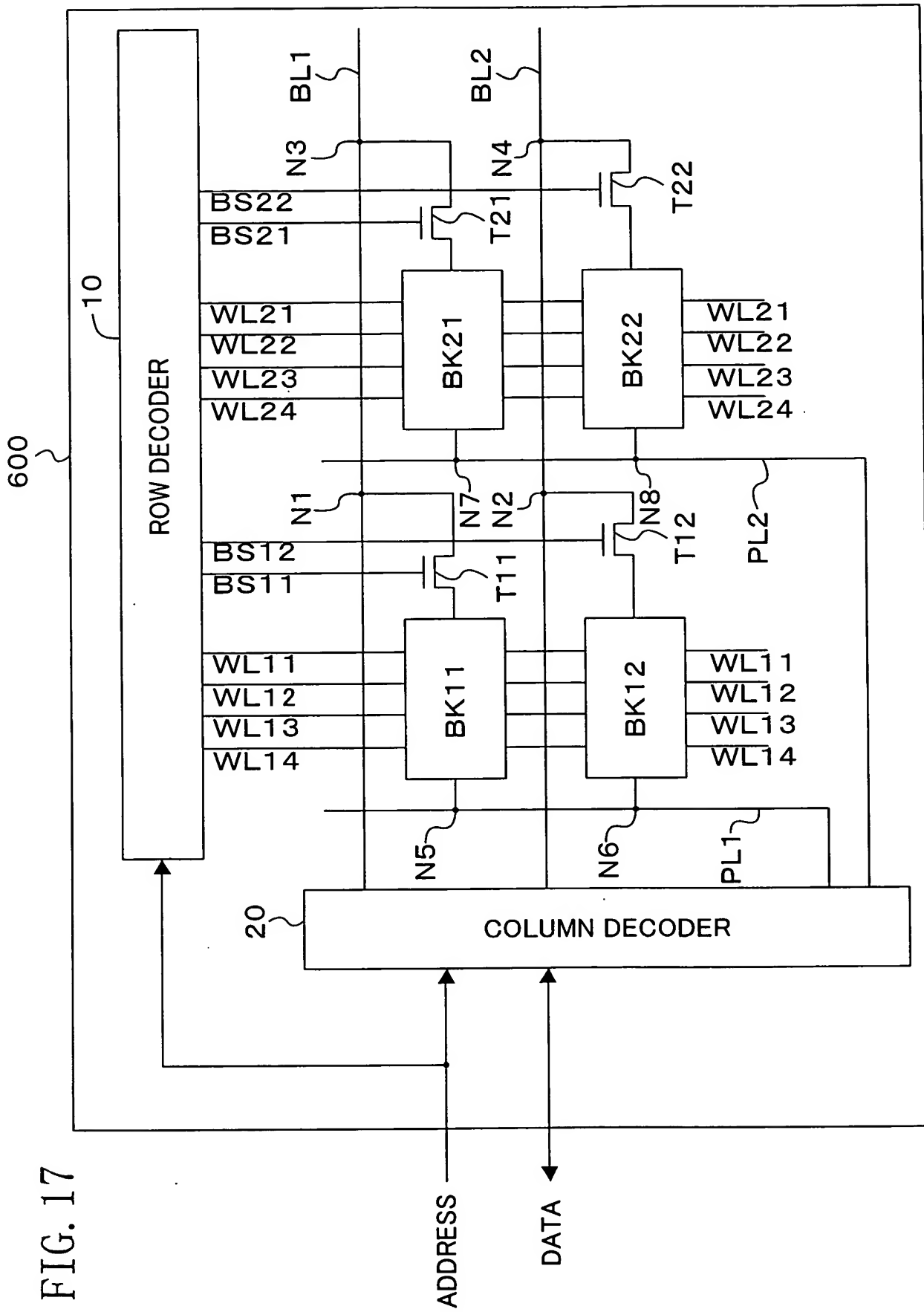


FIG. 18

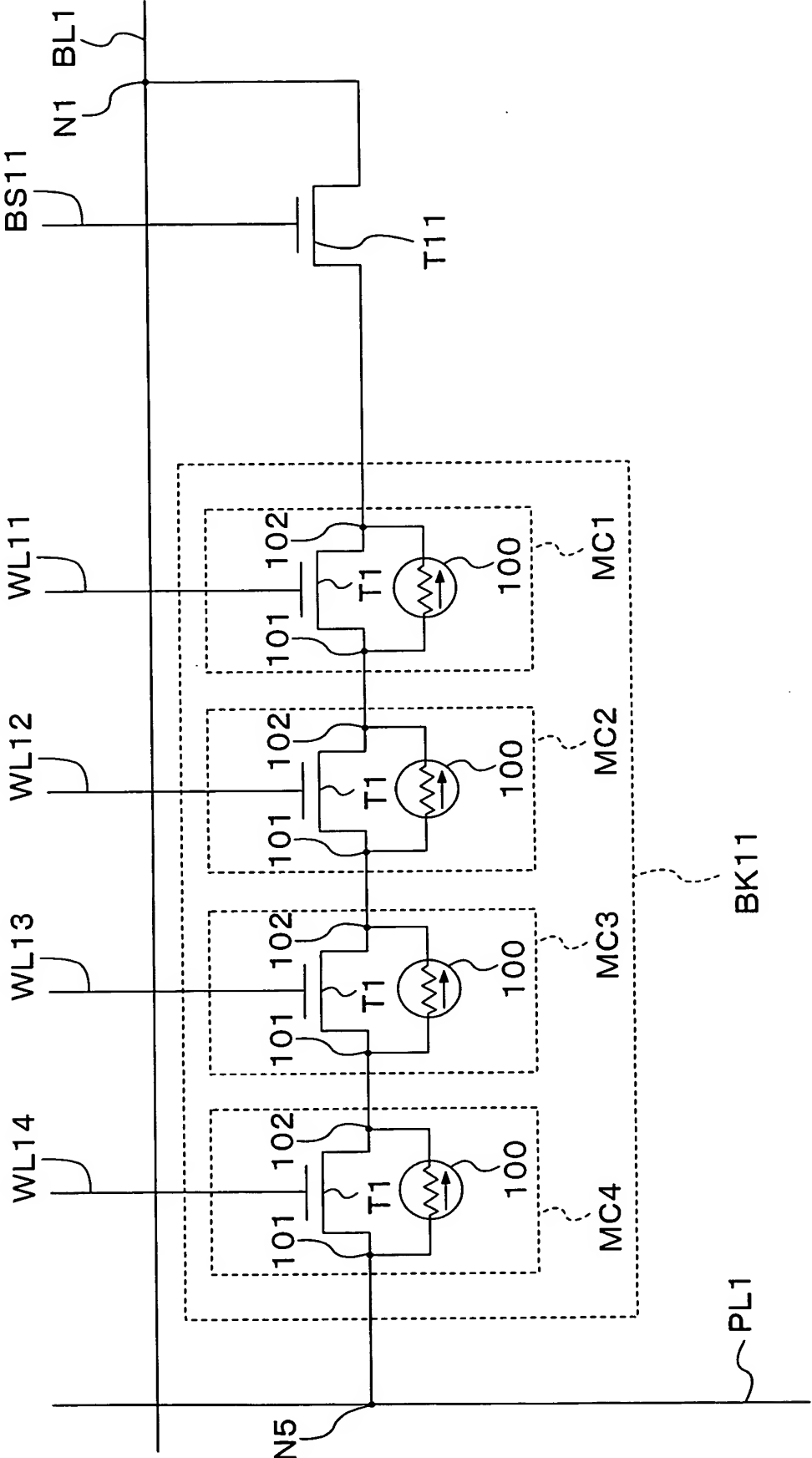
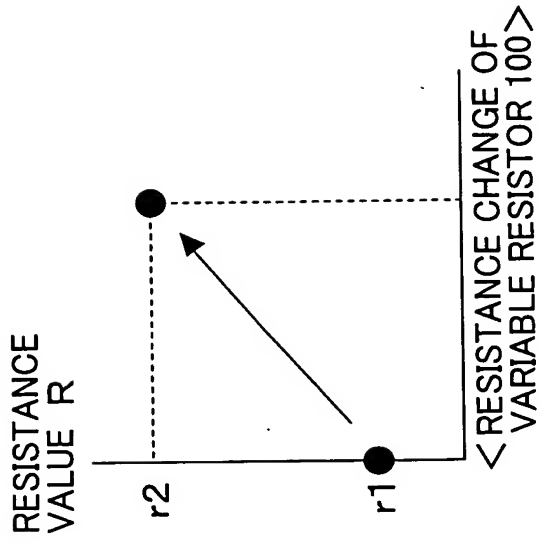
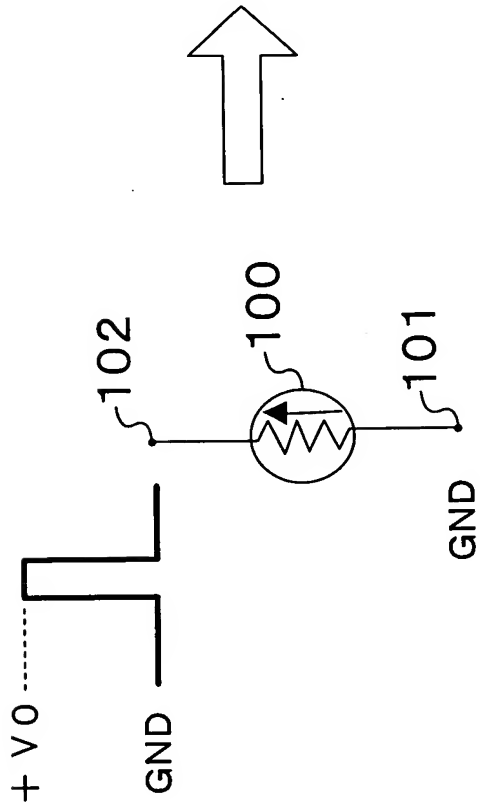
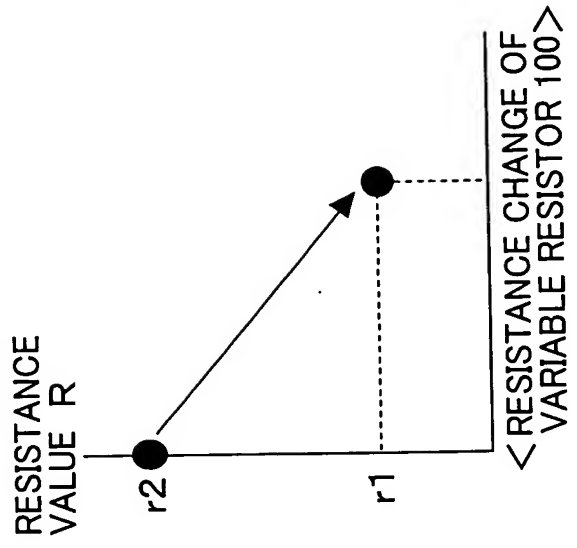
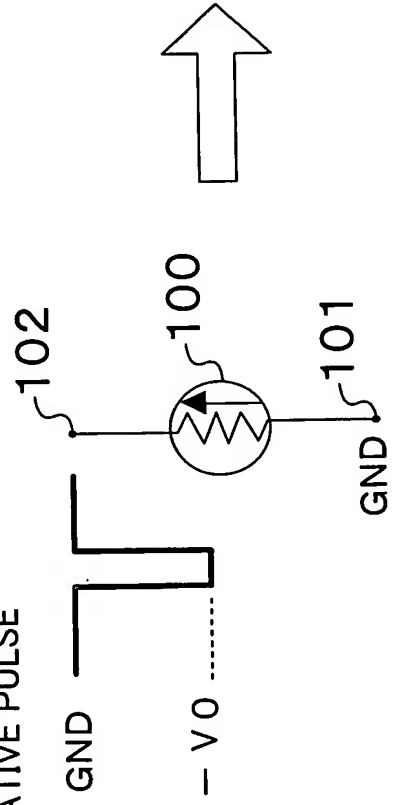


FIG. 19

(a) POSITIVE PULSE



(b) NEGATIVE PULSE



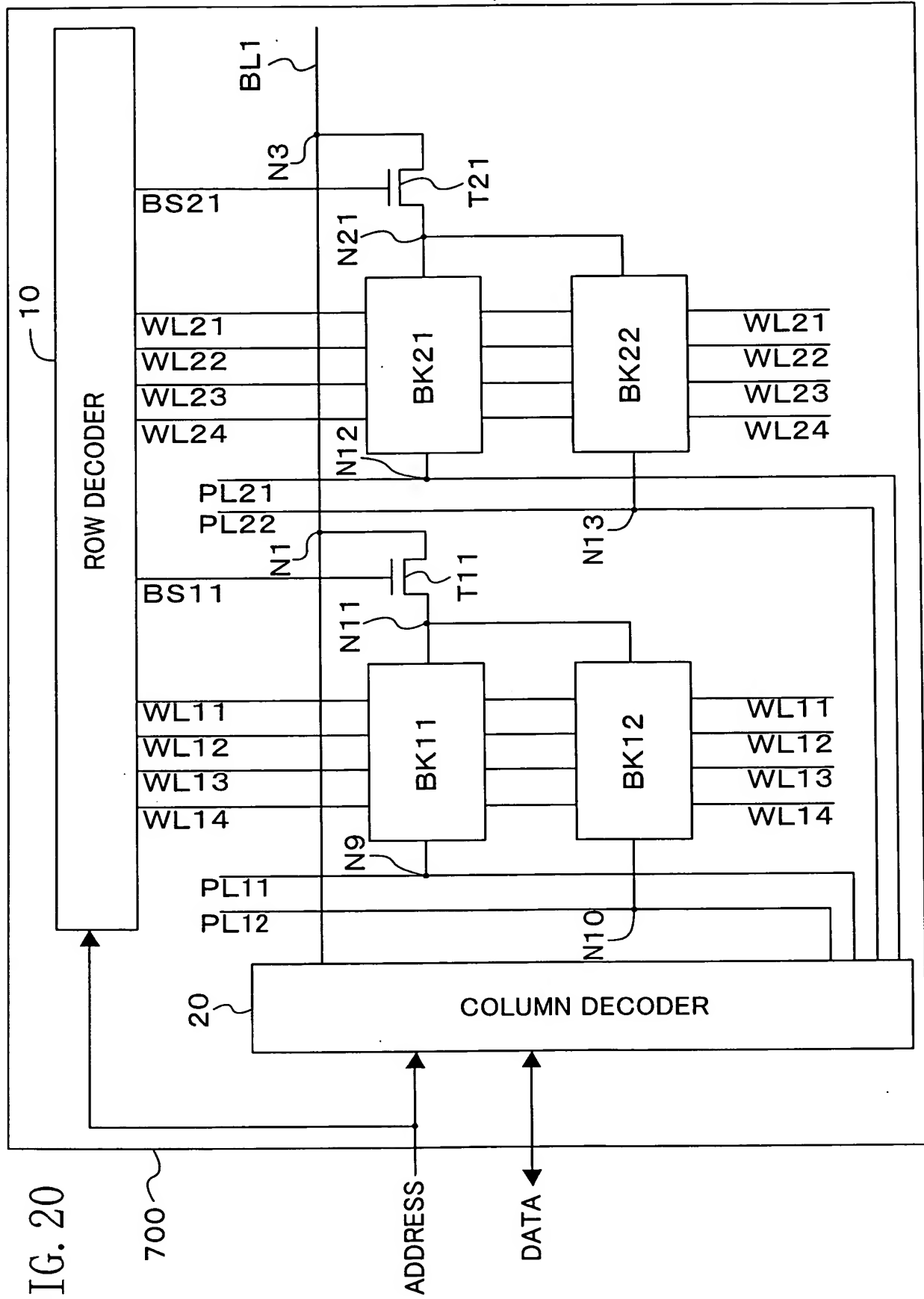




FIG. 21

FIG. 22

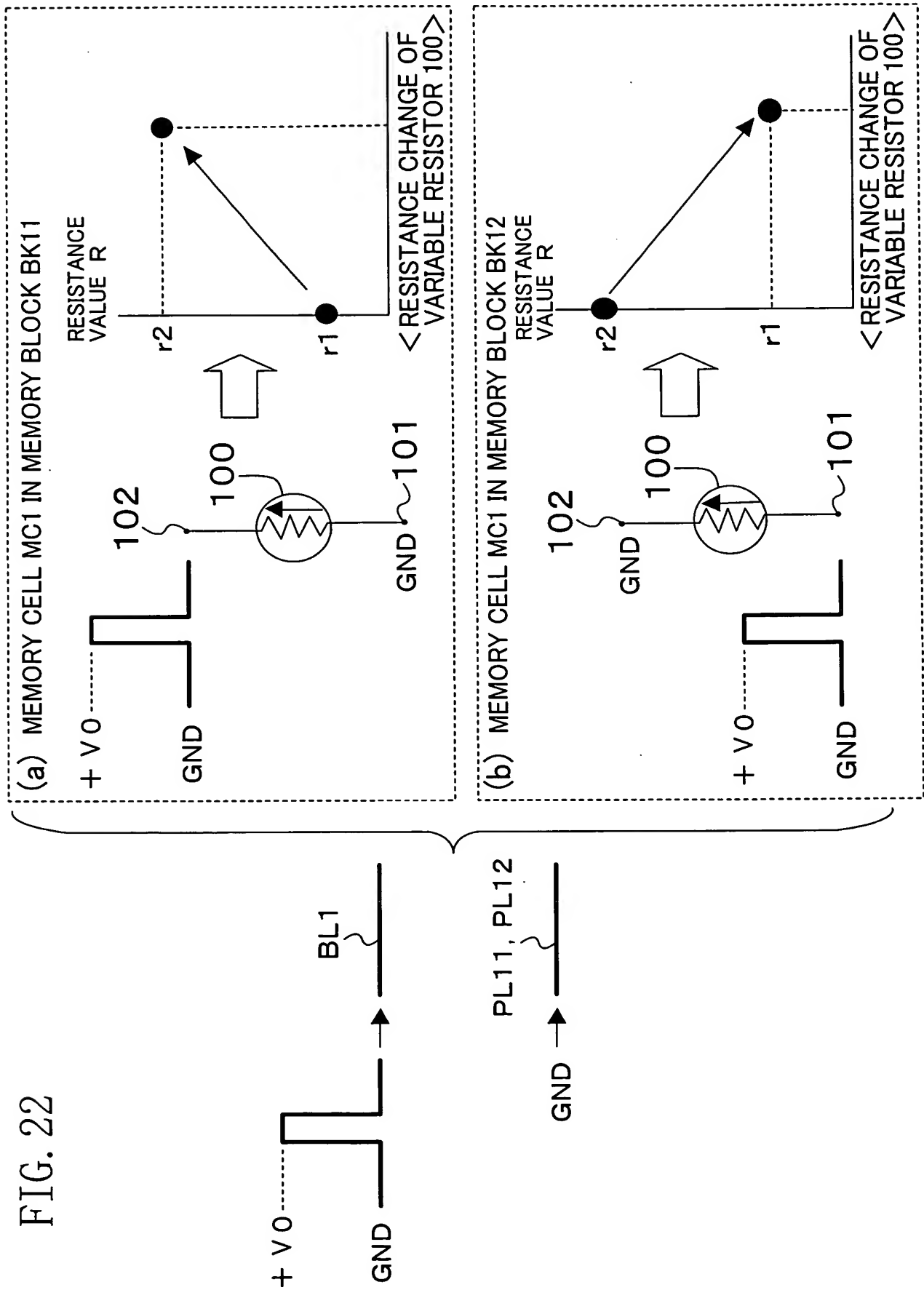


FIG. 23

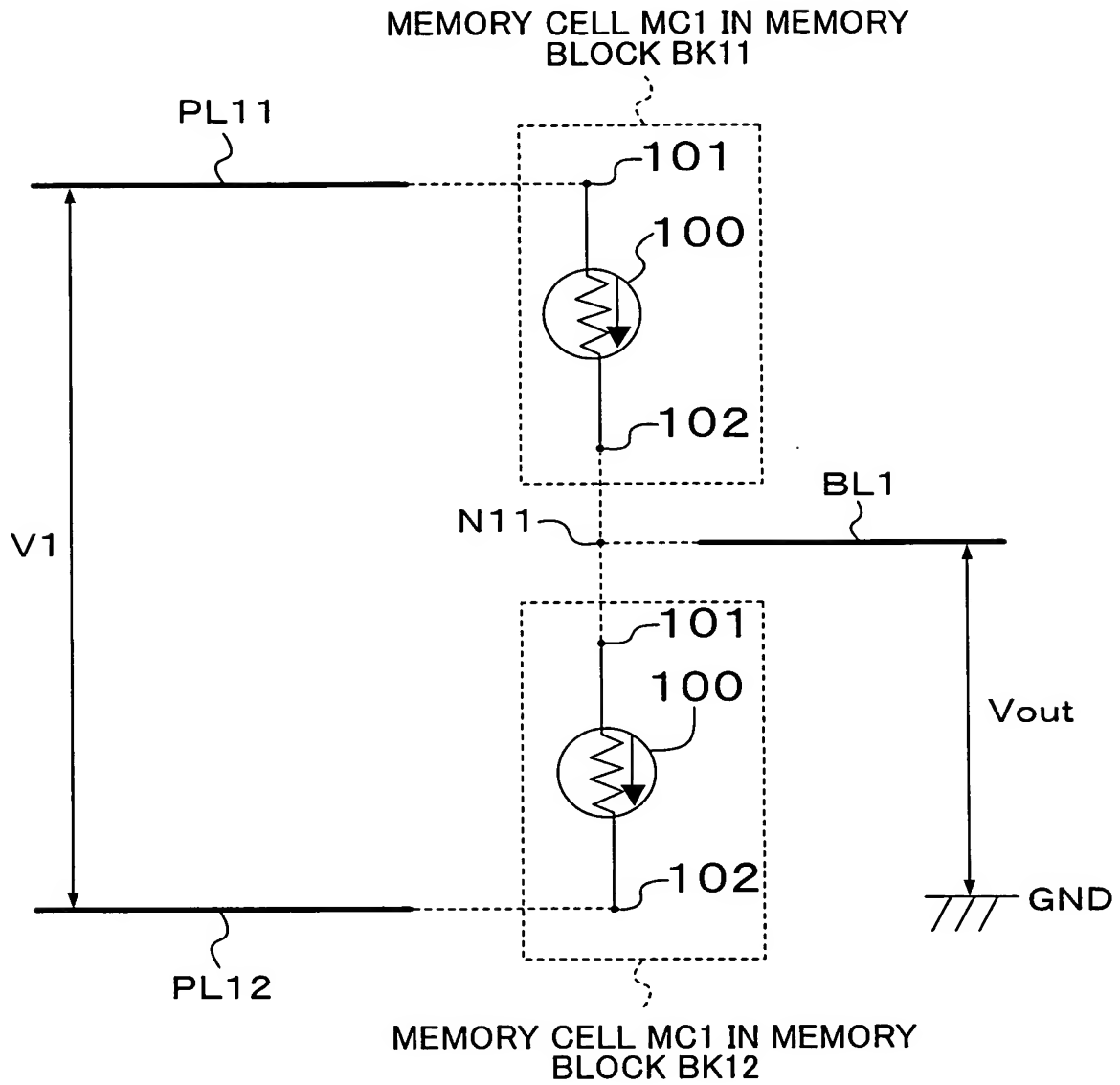
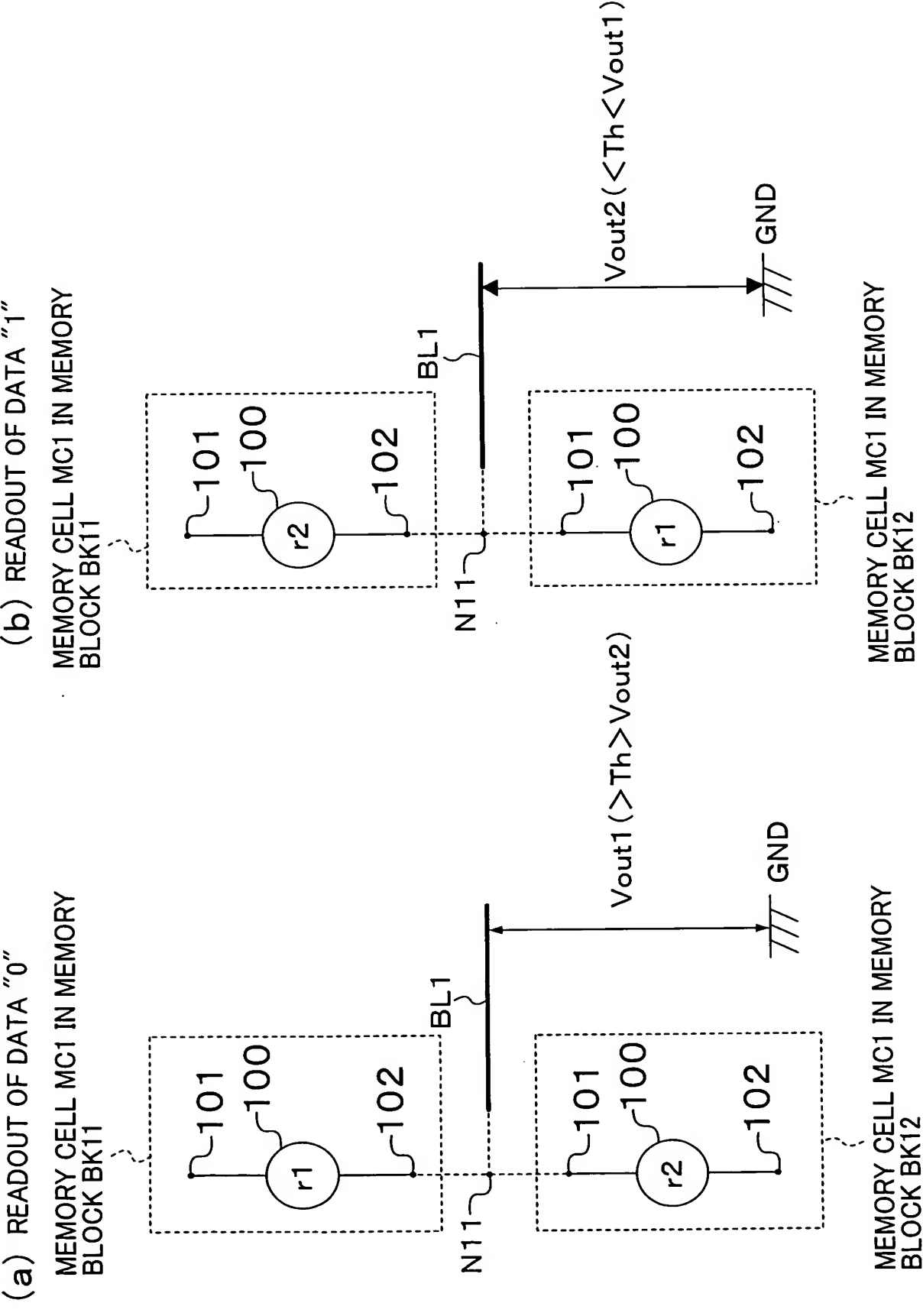
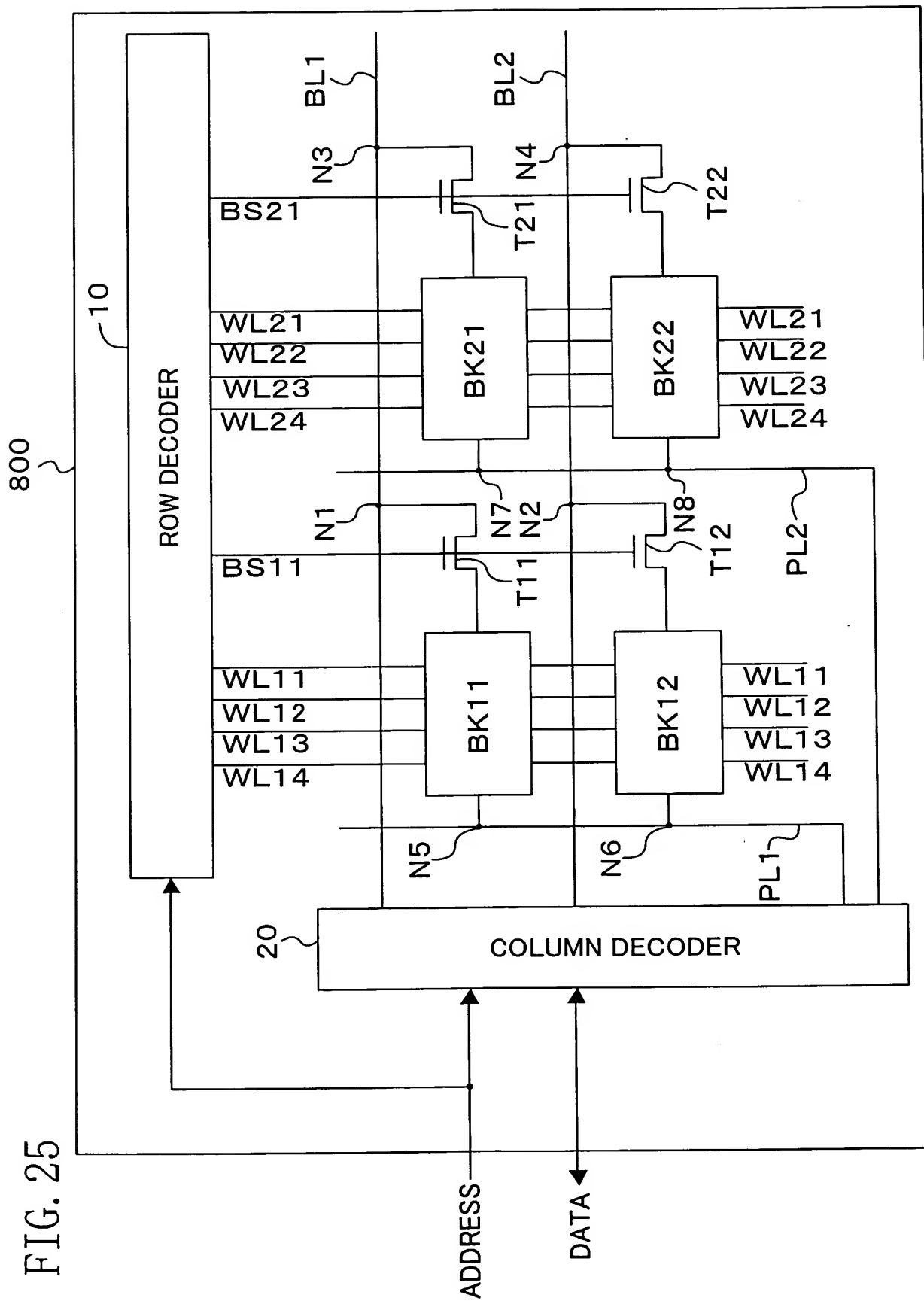


FIG. 24







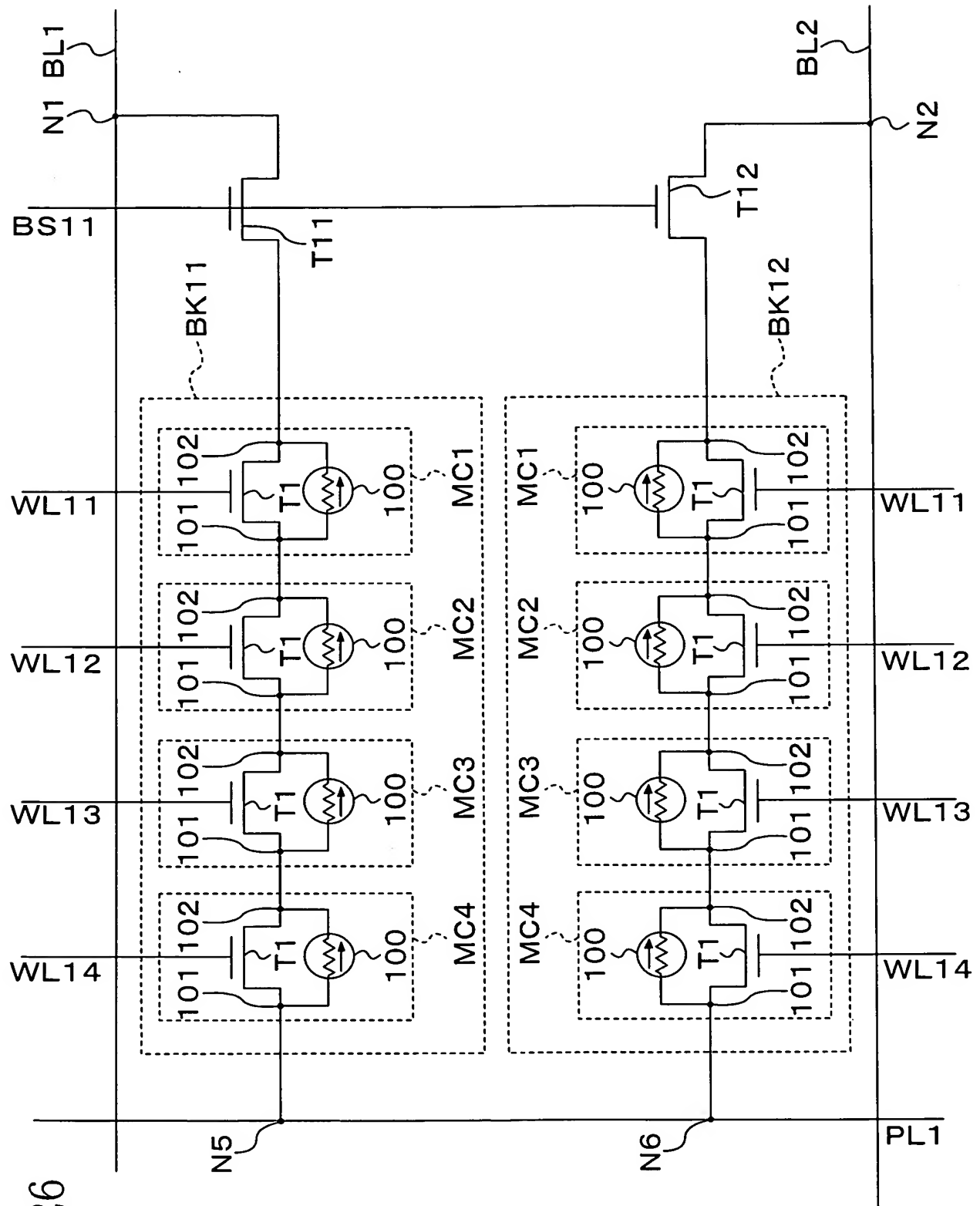


FIG. 26

FIG. 27

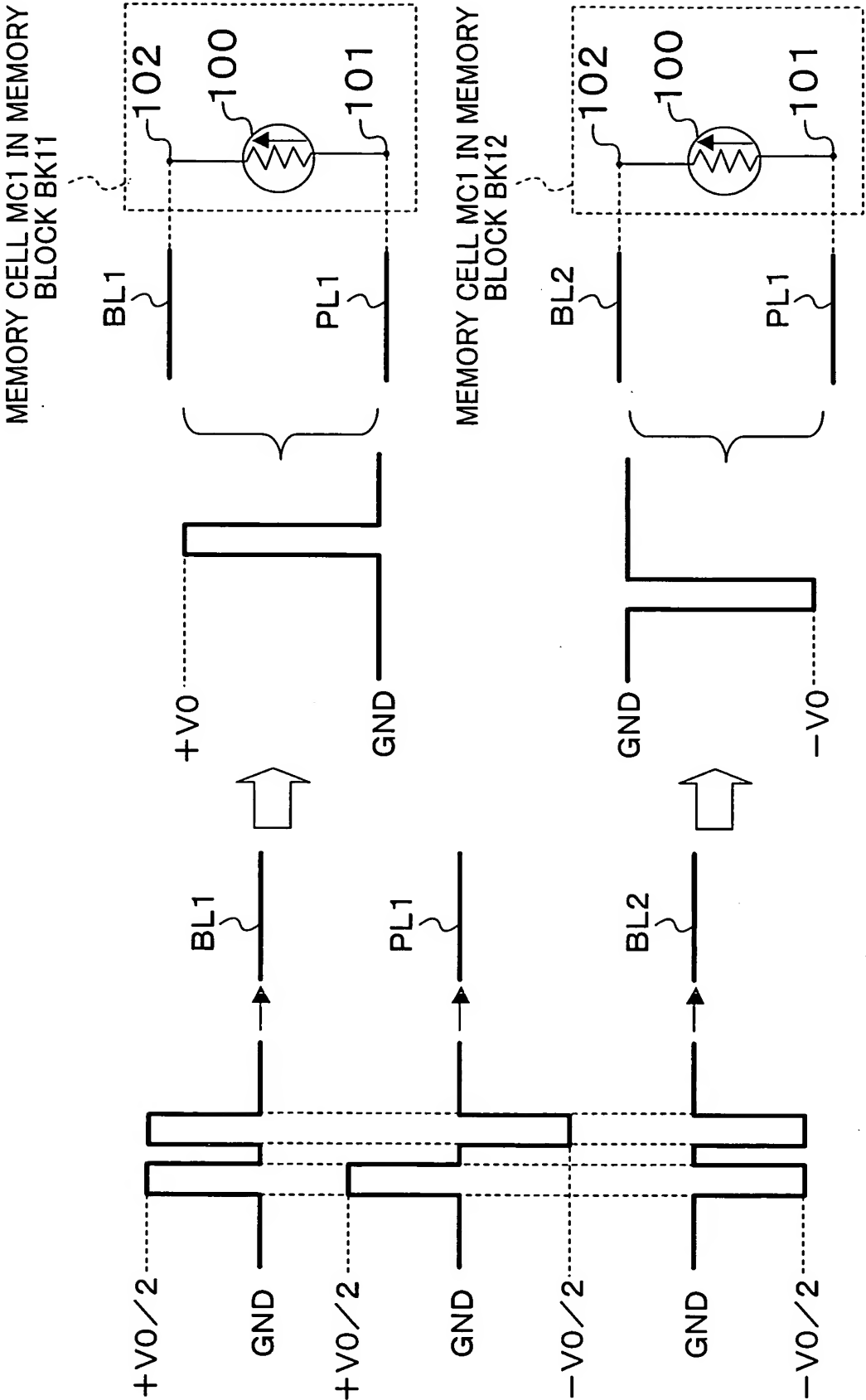


FIG. 28

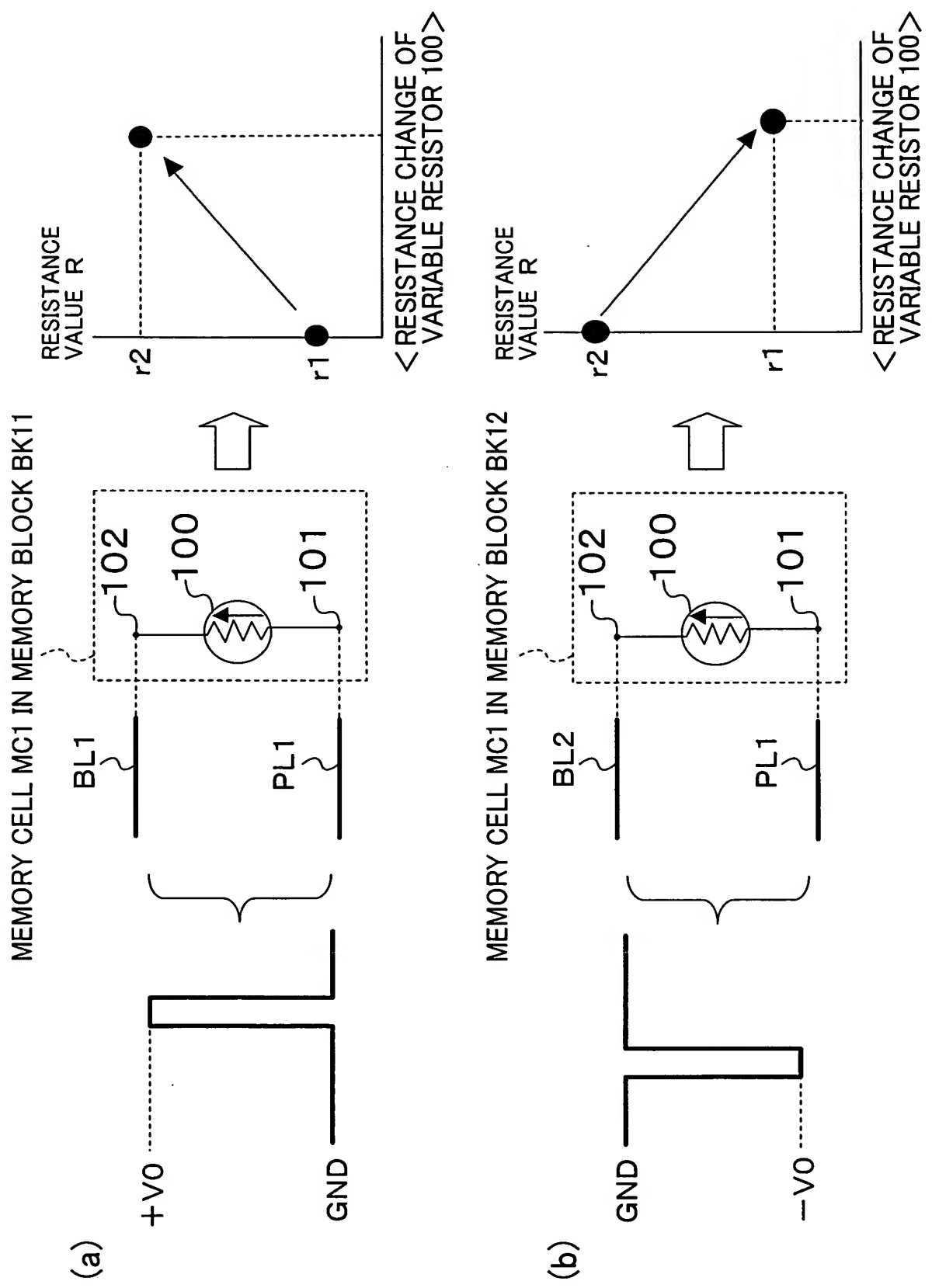
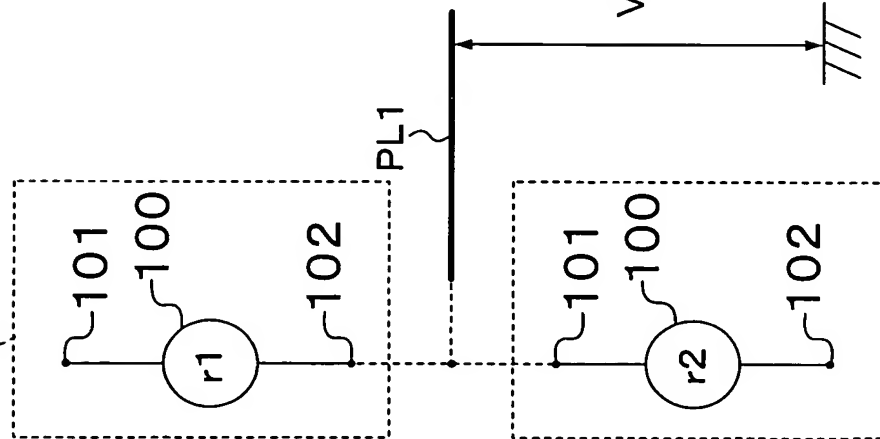


FIG. 29

(a) READOUT OF DATA "0"  
MEMORY CELL MC1 IN MEMORY  
BLOCK BK11



(b) READOUT OF DATA "1"  
MEMORY CELL MC1 IN MEMORY  
BLOCK BK11

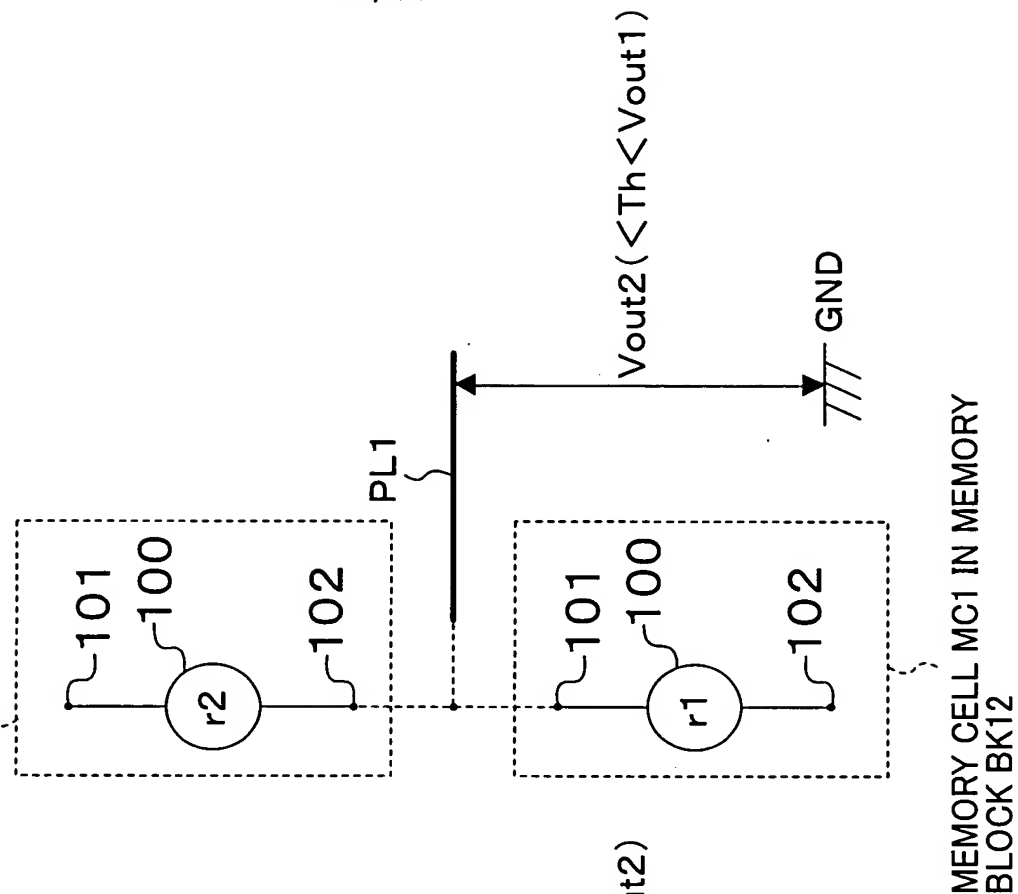


FIG. 30

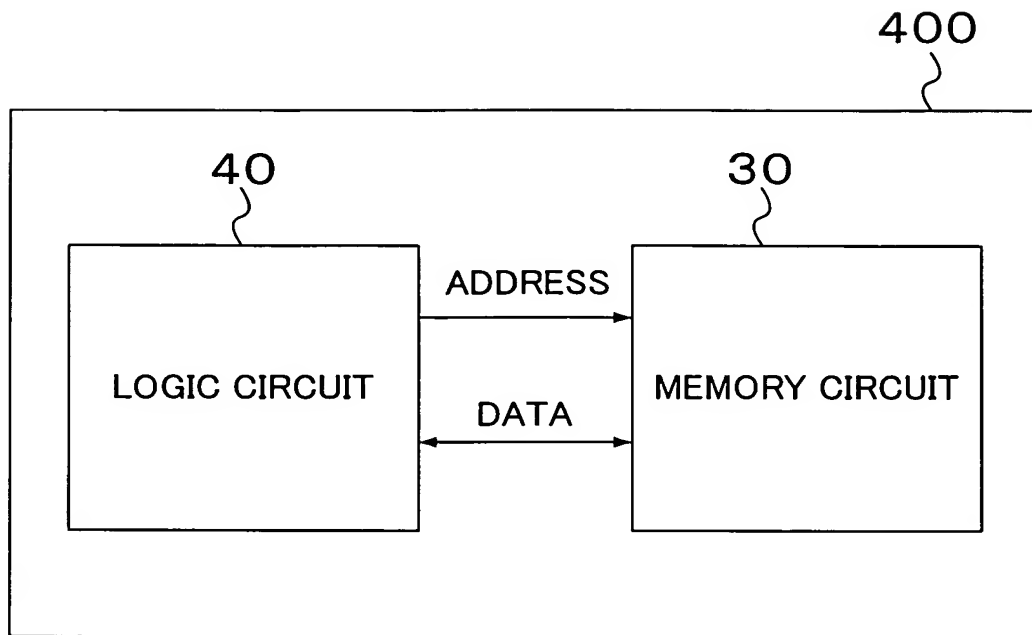


FIG. 31

